50V Driver ASIC

General Description

PD50LE is a linear, differential output, high voltage driver designed to drive capacitive loads such as the TLens® autofocus actuators. The driver has a 10-bit DAC and is capable of 50V DC output voltage controlled by an I2C interface operating at up to 400KHz. A power-on reset circuit guarantees 0V output voltage at start-up and has a power-down feature that reduces current consumption in standby to below 5µA. The ASIC has built-in EMI reduction and is a good fit for EMI sensitive systems where external components are desired to be kept at a minimum.

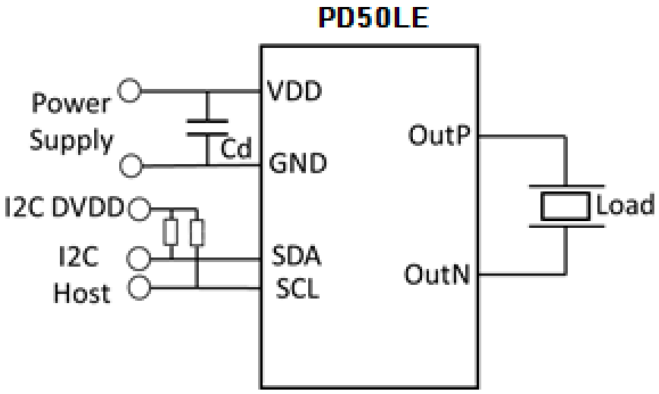
Potential Application Areas

- Smartphones
- Wearables
- Automotive
- Barcode Readers
- Machine Vision
- AR/VR
- Medical instruments
- Webcams

Key Features

- Max output voltage 50V
- Low power consumption (7mW at 50V Vout)
- 3.3V (Standard mode) or 3.5V (Enhanced mode) supply
- Fast transition time with digital control
- 400kHz I2C interface (Fast mode)
- I2C controlled 10-bit DAC
- I2C address 0x18 (Write); 0x19(Read)
- Differential output with selectable polarity
- Status bit indicating target output voltage reached
- 6-pin WLCSP package
- 1.23mm x 0.83mm die area

Application Diagram



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1 Absolute maximum ratings (1)

Parameter	Symbol	Comments	Value	Unit
Max Power Supply Voltage	VDD_{MAX}	Power supply relative to GND	5.5	V
Min Power Supply Voltage	VDD_{MIN}	Power supply relative to GND	-0.3	V
Max OUTP, OUTN output voltage relative to GND	VHV_{MAX}	VDD=3.3V	-0.3/70	V
Max Digital input voltage (I2C)	$DVDD_{MAX}$		5.5	V
Min Digital input voltage (I2C)	$DVDD_{MIN}$		-0.3	V
Current at supply pin	$Ipwr_{MAX}$	Current at VDD and GND	+/-30	mA
Current at other pins	$Ipin_{MAX}$		+/-5	mA
Extended operation temperature	T_{extOp}	Power Applied	-55/+125	°C
Storage temperature	T_{STG}	No Power Applied	-65 to +150	°C
Lead temperature (soldering 10s)	T_{LEADS}	JEDEC J-STD-020	+260	°C
Latchup current (VDD, SCL, SDA balls)	I_{LUP}	JESD78D, Class I	+/-100	mA
Latchup current (OUTP and OUTN balls)	I_{LUP}	JESD78D, Class I	+/-50	mA
ESD protection all pins	HBM	Human Body Model JESD22-A115-A114 Class2	2	kV

Table 1 Absolute Maximum Ratings

(1) Absolute maximum ratings are limiting values (referenced to GND=0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. Applying conditions above absolute maximum ratings may be destructive to the devices.

Remark: Refer to § 5.1 Output Voltage Control for safe operation of the driver

2 Recommended operating conditions

Parameter	Symbol	Comments	Min.	Nominal	Max.	Unit
Power supply	V_{DD}	Standard performance	3.2	3.3	3.4	V
Power supply	V_{DD}	Enhanced performance	3.4	3.5	3.6	V
Digital input voltage (I2C)	$DVDD_{OP}$	I2C DVDD supply	1.7	1.8	3.6	V
Operating temperature	Top		-25	25	85	˚C
Analog Supply rise time	T_{VDD}		0.001	-	30	ms

Table 2 Recommended operating conditions

2.1 Operating modes

PD50 can be operated in two different modes: calibrated mode and max DAC mode. The calibrated mode will take advantage of the full voltage range for each driver device, while the standard max DAC mode operates with a maximum allowed DAC that will be writeable for all devices under all operating conditions.

The trade-off between the two modes is additional software logic versus voltage range. The max DAC mode has a slight decrease in voltage operating range and the calibrated mode requires some additional software logic. Please refer to chapters 5.6 MAX_DAC parameter and 5.7 MAX_DAC calibration for detailed explanation.

3 Electrical characteristics

Unless precise, Min/Max parameters apply to operating temperature range

3.1 Standard performance, 3.3V supply voltage

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DAC output performance					
Maximum voltage CALIBRATED_MODE [1]	$VOUT_{MAX}$	48	49		V
Maximum guaranteed DAC code [2]	MAX_DAC	875			
Maximum voltage MAX_DAC_MODE	$VOUT_{MAX\_DAC}$	47	48		V
DAC LSB step (referred to output)	V_{LSB}	53	55	57	mV
Common-mode output offset voltage in active state	V_{CM}		1.85		V
Output differential in standby state	$VOUT_{STBY}$		0		V
DAC resolution	DAC_{RES}		10		bits
Differential Output (OUTP-OUTN) Nonlinearity [3]	DNL	-4	+/- 0.9	4	LSB
Differential output Integral Nonlinearity	INL	-6	+/- 3	6	LSB
Differential output Zero-code offset [4]	$DAC0_{OFFS}$	-240	0	240	mV
Vout_lock trigger voltage (positive or negative)	V_{LOCK_DIFF}		0.65		V
VOUT variation over operating temperature range	OUT_{TV}		0.05	0.25	%
Charge pump rise time 0-40V [5]					
Load = TLens® Silver Premium	TR_{40V}		2.3		ms
Load = TLens® Silver	TR_{40V}		3.1		ms
Load = 33 nF, 100V capacitor	TR_{40V}		3.3		ms
Output load					
Capacitive Load	C_{LOAD}	5	30	100	nF
Resistive Load	R_{LOAD}	100			MΩ
Current sink fall time 40-0V[6]					
Load = TLens® Silver Premium	T_{40V-0V}		1.1		ms
Load = TLens® Silver	T_{40V-0V}		1.5		ms
Load = 33 nF, 100V capacitor	T_{40V-0V}		1.8		ms
Power Consumption					
Power Consumption in standby mode	I_{SB}	0.05	0.25	5	µA
Active supply current, Vout < 28V, VDD=3.3V	IDD_{LV}		1.0	2	mA
Active supply current, Vout > 28V, VDD=3.3V	IDD_{HV}		1.5	3	mA
Maximum supply current during load charging [7]	IDD_{CHG}		15	22	mA
Power-On start-up delay					
Delay from power on to first valid I2C access [8]	T_{POD}	15	30	75	ms
I2C specification					
Low level input threshold SDA, SCL	V_{IL}			0.5	V
High level input threshold SDA, SCL	V_{IH}	1.2			V
Low level output voltage SDA (Sink 3mA)	V_{OL}	0		0.3	V

Table 3 : Standard electrical Characteristics

3.2 Changed electrical characteristics enhanced performance, 3.5V supply voltage

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DAC output performance					
Maximum voltage CALIBRATED_MODE [1]	$VOUT_{MAX}$	51	52		V
Maximum guaranteed DAC code [2]	MAX_DAC	920			
Maximum voltage MAX_DAC_MODE	$VOUT_{MAX\_DAC}$	50	51		V
Charge pump rise time 0-40V[5]					
Load = TLens® Silver Premium	TR_{40V}		2		ms
Load = TLens® Silver	TR_{40V}		2.9		ms
Load = 33 nF, 100V capacitor	TR_{40V}		3.5		ms

Table 4 : Enhanced electrical Characteristics

Notes:

1. Maximum guaranteed DAC code can be increased by device calibration. Please refer to chapter 5.7 for details.
2. Highest DAC code reachable is guaranteed for 0 to 70 °C operating temperature as well as for other under worst-case operating conditions. Please refer to chapter 5.6 for details.
3. Largest DNL error occurs between DAC=511 and DAC=512.
4. When the polarity changes, the $DAC0_{OFFS}$ voltage changes polarity, resulting in a Vout step of $2*DAC0_{OFFS}$.
5. 10% to 90% rise time
6. 90% to 10% fall time
7. Max supply current during charging of load, typically 1-5ms duration depending on VOUT step size.
8. Delay measured from time when VDD reaches operating voltage.

4 I2C

4.1 Register map

Address	Name	Description	Bits	Default	Type
0x0	MODE	Function control register	[3:0]	0x00	RW
0x1	Reserved		[5:0]	0x28	RW
0x2	DAC_MSB	DAC value (MSB)	[7:0]	0x00	RW
0x3	DAC_LSB	DAC value (LSB)	[7:0]	0x00	RW
0x4	STATUS	Provides error & status information	[1:0]	0x00	RO
0x5	Reserved		[7:0]	0x00	RO
0x6	Reserved		[7:0]	0x00	RO
0x7	CHIP_ID	Revision id of the die	[7:0]	0xA2	RO

Table 5 :PD50 Register Map

4.2 Register format

The format for registers at address 0x0 to 0x7 is given below. All multi-bit fields are aligned with LSB at position 0. Writing to Read-Only (RO) bit fields has no effect.

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0	MODE								ENABLE
0x1	RESERVED								
0x2	DAC_MSB	POL_SEL						DAC[9:8]	
0x3	DAC_LSB	DAC[7:0]							
0x4	STATUS							DAC_ERRLTCH	VOUT_LOCK
0x5	RESERVED								
0x6	RESERVED								
0x7	CHIP_ID	CHIP_ID[7:0]							

Table 6: Register Address map

Address 0x0	**MODE**			
Bits	**Name**	**Mode**	**Default**	**Description**
7..3	Reserved	RO	0x0	
2..1	Reserved	RW	0x0	Reserved, keep default value
0	ENABLE	RW	0x0	1: PD50 active 0: PD50 in standby

Table 7: MODE register format

Address 0x2	**DAC_MSB** (Register write does not have any effect on Vout until DAC_LSB is written)			
Bits	**Name**	**Mode**	**Default**	**Description**
7	POL_SEL	RW	0x0	Polarity selection 1: Positive polarity; OutP ≥ OutN 0: Negative polarity: OutP ≤ OutN
6..2	Reserved	RO	0x00	Not used
1..0	DAC[9:8]	RW	0x0	MSB of DAC

Table 8 :DAC_MSB register format

Address 0x3	DAC_LSB (Register write will update DAC_MSB and DAC_LSB to voltage control system)			
Bits	**Name**	**Mode**	**Default**	**Description**
7..0	DAC[7:0]	RW	0x00	LSB of DAC.

Table 9: DAC_LSB register format

Address 0x4	STATUS			
Bits	**Name**	**Mode**	**Default**	**Description**
7..2	Reserved	RO	0x00	
1	DAC_ERRLTCH	RW	0x0	Dac Write Error latch. Write 0 to STATUS register to reset latch. 1: DAC_LSB write while VOUT_LOCKED=0. 0: No Dac write error event since last write.
0	VOUT_LOCK	RO	0x0	1: Output voltage within +/-V_{LOCK_DIFF} range. 0: Output voltage in transition state

Table 10: STATUS register format

Address 0x7	CHIP_ID			
Bits	**Name**	**Mode**	**Default**	**Description**
7..0	CHIP_ID	RO	0xA2	Revision ID for PD50.

Table 11: CHIP_ID register

4.3 Interface

The host controls the PD50 through the I2C registers. At power-on the default values are loaded into the registers. Setting the device in reset mode will reload the default values. The 7-bit slave address is 0xC (0b0001100). The LSB of the address byte is the R/W indicator, so that I2C write operations is done at slave address 0x18, and I2C read operations is done at slave address 0x19.

4.4 Transaction format

The I2C interface supports single-byte access and burst-mode access. Read operations may be done from the current register address or from a random address. Note that the address pointer is always incremented after a read or write access. For example, after writing the DAC LSB register at register address 0x3 the status register at address 0x4 can be read using a sequential read from current address.

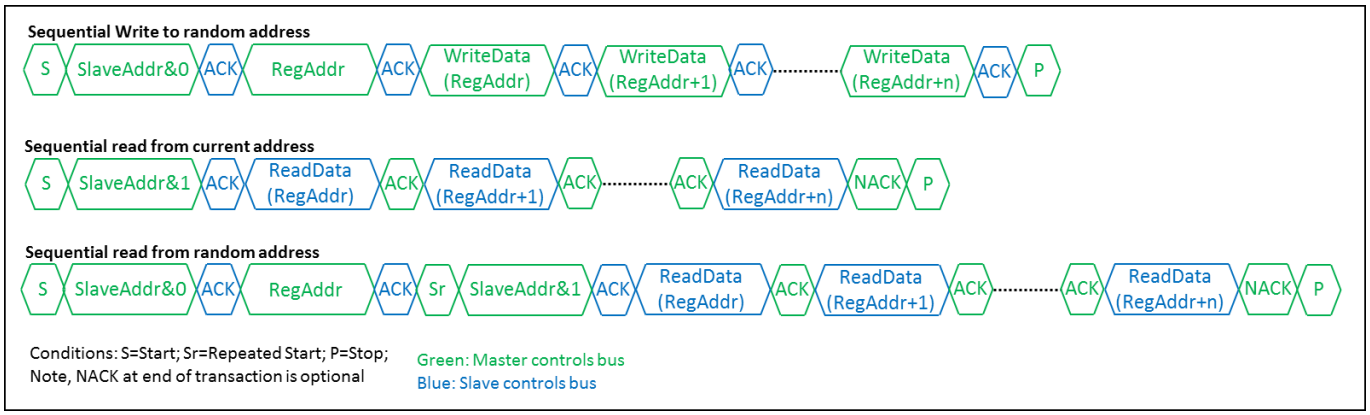

Figure 1 : I2C transaction format

4.5 Timing specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
I2C timing specification					
Maximum SCL clock frequency	f_{SCL}	0	100	400	kHz
SCL clock low time	t_{LOW}	1.3			µs
SCL clock high time	t_{HIGH}	0.6			µs
I2C rise time	t_r	20		300	ns
I2C fall time	t_f	7		300	ns
Data setup time	$t_{SU;DAT}$	100			ns
Data hold time	$t_{HD;DAT}$	0			ns
Repeated start condition setup time	$t_{SU;STA}$	0.6			µs
Start condition hold time	$t_{SU;HD}$	0.6			µs
Stop condition setup time	$t_{SU;STO}$	0.6			µs
I2C free time between stop and start conditions	t_{BUF}	0.5			µs
Data Valid time (from SCL LOW to SDA output HIGH or LOW)	$t_{VD;DAT}$			0.9	µs
Data Valid Acknowledge time (from SCL LOW to SDA output HIGH or LOW)	$t_{VD;ACK}$			0.9	µs
Spike suppression width	t_{SP}	50			ns

Table 12: I2C timing parameters

Please refer to UM10204 for additional I2C timing explanation.

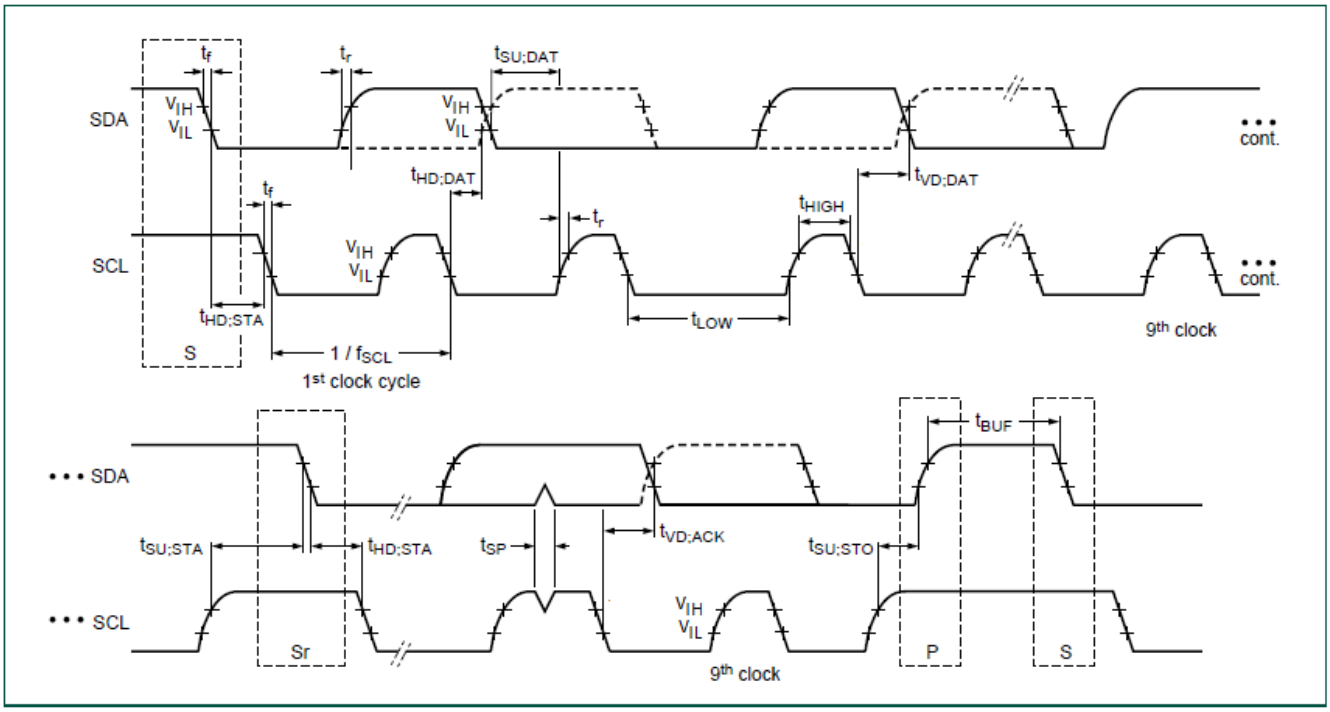

Figure 2 : I2C timing parameter definition

5 Theory of operation

The PD50 is a fully integrated capacitive load driver solution with I2C interface, DAC, charge pump, current sink and associated logic with control and status registers. The load can be driven up to +/- OUT_{MAX} .

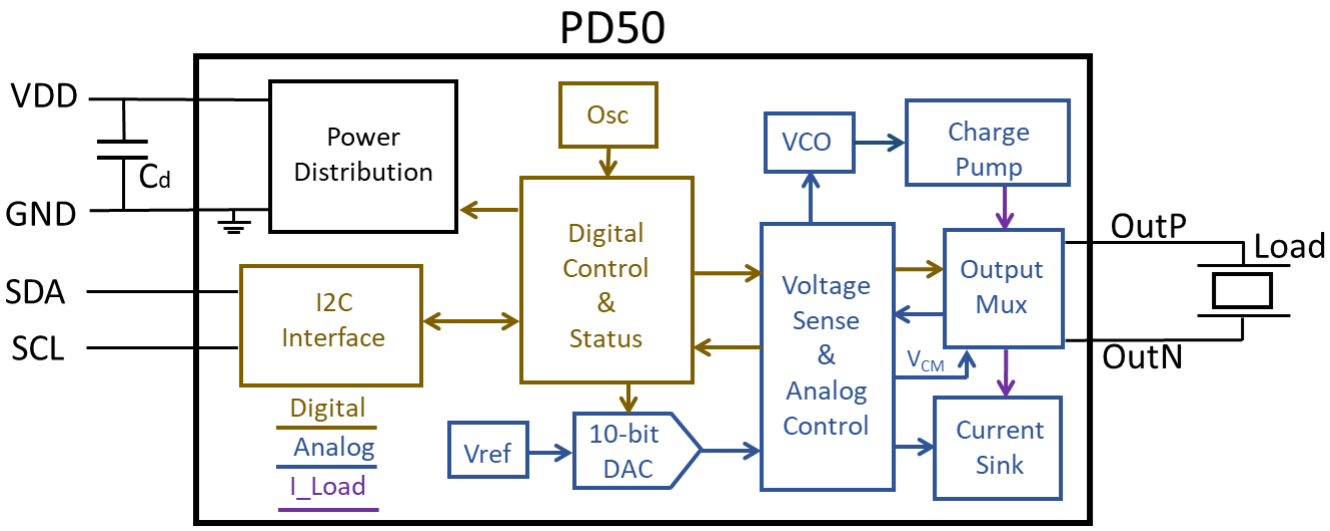

Figure 3 PD50 Functional block diagram

5.1 Output Voltage Control

The load is connected between the OutP and OutN terminals. The load is charged by the charge pump and discharged via the current sink. The voltage sense unit continuously monitors the output voltage via an attenuator and compares with the DAC output voltage. The voltage sense keeps the output voltage at the target voltage by charging/discharging the load as required. It is necessary to have at least $C_{LOAD(MIN)}$ connected to the output when the PD50 is active. As the capacitive load is increased, the Vout slew rate will decrease.

Important remark: Note that, when the load is still charged, disconnecting the power supply might cause the load to discharge across the OUTP and OUTN balls, resulting in an injection current that may damage the device. This can be avoided by writing zero to the enable register before switching off the power supply, putting the driver on standby mode and discharging the load accordingly. Refer also to application note, available on demand, for further application and implementation information.

5.2 Power-on startup delay

When PD50 is powered on, there is an internal delay T_{POD} before any I2C access is responded. Any I2C access during this period has no effect, and the ACK bit will not be cleared.

5.3 Output Voltage transfer function

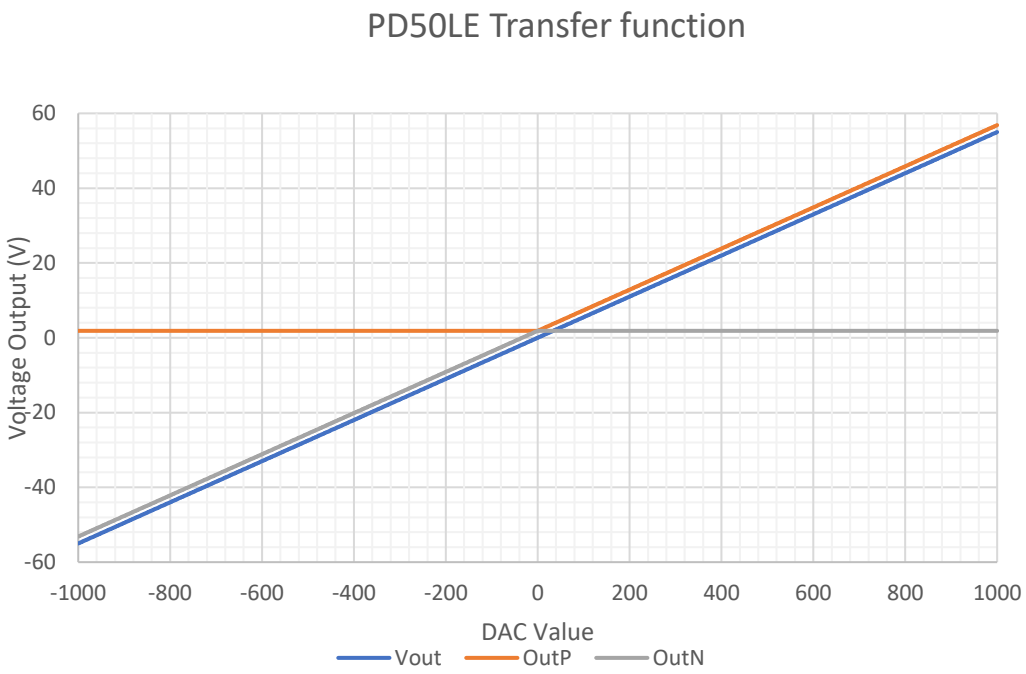

Figure 4 PD50 Transfer function

The output is connected to the load in differential mode.
The output is connected to the load in differential mode and given by the formula:

$$|V_{out}| = |V_{OUTP} - V_{OUTN}| = N_{DAC} * V_{LSB}$$

$$Positive\ output: POL_{SEL} = 1 \rightarrow OUT_P \geq OUT_N$$

$$Negative\ output: POL_{SEL} = 0 \rightarrow OUT_P \leq OUT_N$$

When PD50 is active, OutP and OutN have a constant common-mode voltage V_{CM} referred to GND. The common mode voltage has a typical value of 1.85V.
When PD50 is in standby mode, both OutP and OutN are pulled to GND via a MOS transistor.

5.4 Transition timing; VOUT_LOCK status bit

When DAC_LSB is written, the contents of the DAC_MSB and DAC_LSB registers are latched to the DAC, and the VOUT_LOCK status bit is cleared if the new DAC voltage is more than V_{LOCK_DIFF} away from the current output voltage. When $|V_{OUT}-V_{TARGET}| \leq V_{LOCK\_DIFF}$ the VOUT_LOCK status bit will be set. The transition is finished when the VOUT_LOCK status bit is set. When the transition is less than V_{LOCK_DIFF}, it is considered finished immediately after the DAC_LSB register is loaded. The VOUT_LOCK bit will not change state during such a transition.

5.5 DAC write while transition is on-going

If new DAC=0, the on-going transition will be aborted and the transition to DAC=0 will immediately start. When the transition to 0 is complete, VOUT_LOCK will be set as in a normal transition. If new DAC ≠ 0, the new value is ignored. The on-going transition will not be affected, and VOUT_LOCK will be set when the transition is complete. At this point the host can reactivate the transition by writing to DAC_LSB. In both cases the status bit DAC_ERRLTCH will be set. The DAC_ERRLTCH is latched and is reset by writing 0 to the STATUS register.

5.6 MAX_DAC parameter

The MAX_DAC parameter is defined as the highest DAC value for which the lock bit is guaranteed to be set under worst-case operating conditions. If the value loaded into the DAC register is higher than MAX_DAC, it is possible that the VOUT_LOCK status bit will never be set. In this case, the charge pump will run continuously, any further non-zero value written to the DAC register will be ignored, and the output voltage will be lower than the target voltage. To avoid this situation, the host software should enforce that the DAC is never loaded with a value higher than MAX_DAC. The MAX_DAC violation condition can be detected by polling the VOUT_LOCK bit. If the VOUT_LOCK bit is not set within a timeout limit, normal operation can be resumed by writing 0 to the DAC register (DAC_MSB=0 and DAC_LSB=0).

5.7 MAX_DAC calibration

Operating in calibrated mode can be useful when the full voltage range for each driver device is required. To calibrate the MAX_DAC for a specific device the host software can write DAC code = MAX_DAC (870 in normal mode and 910 in enhanced mode). Then keep increasing the DAC value by 1 and poll the VOUT_LOCK bit after 5 ms until VOUT_LOCK ≠ 0. If VOUT_LOCK = 0 after 5 ms, the calibrated MAX_DAC is then the current DAC value – 1. Store the MAX_DAC value in EEPROM or similar, then proceed operation at the full voltage range with the new MAX_DAC code. Note that the maximum achievable DAC can be affected by supply voltage and temperature. If there is a decrease in temperature or supply voltage, the MAX_DAC may need to be recalibrated. A good practice can be to poll the VOUT_LOCK bit whenever writing DAC values greater than the default MAX_DAC.

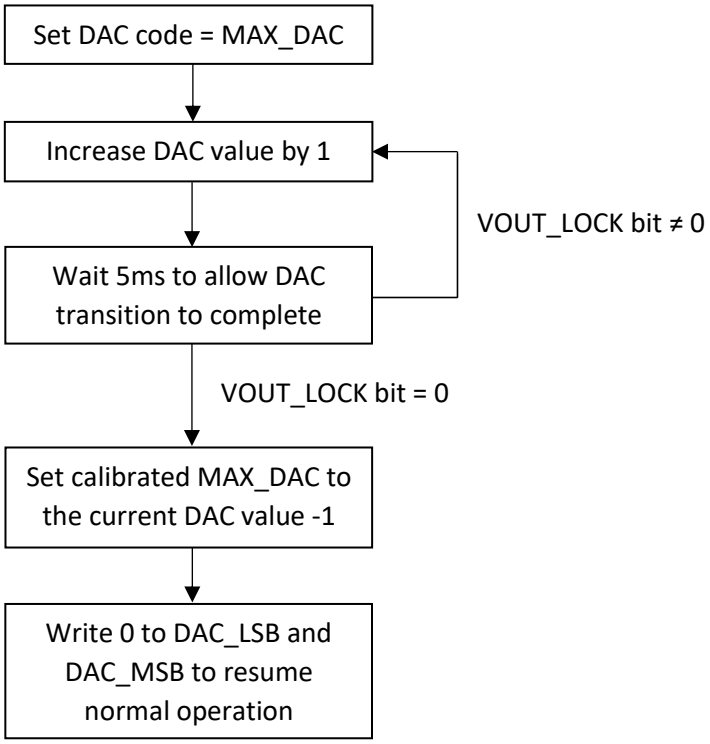

Figure 5 : MAX_DAC calibration block diagram

5.8 Polarity change

If a new DAC value write contains a polarity bit change, the output voltage will first go to zero (OutP=OutN) before polarity change takes place. Thereafter the output voltage will transit to the final value.

5.9 Standby mode

In standby mode the power consumption of PD50LE drops to I_{SB}.
The PD50 can be put in standby mode by the following sequence:

1. Write 0 to the DAC_MSB and DAC_LSB registers.
2. Write 0 to the ENABLE bit in the MODE register.

6 Package

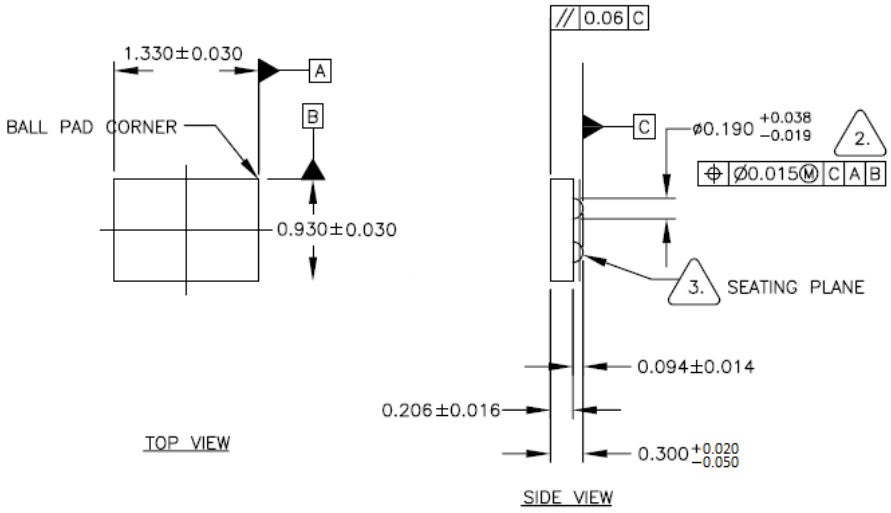

Figure 6 : Package Description (all dimension in mm)

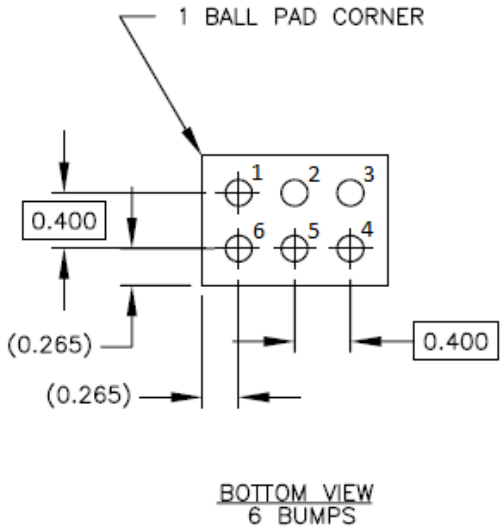

Figure 7 Ball layout (all dimensions in mm)

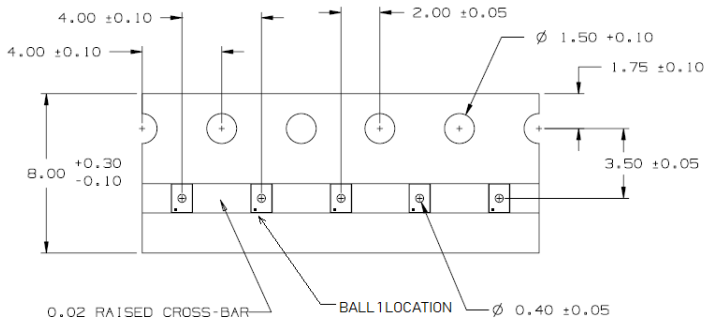

Figure 8 Tape layout (dimensions in mm)

6.1 Ball description

Symbol	Ball	Type	Function
VDD	2	Supply	Power supply input
GND	5	Supply	Ground
SCL	1	I	I2C bus clock input
SDA	3	I/O	I2C bus data input/output
OUTP	6	O	Positive high voltage output
OUTN	4	O	Negative high voltage output

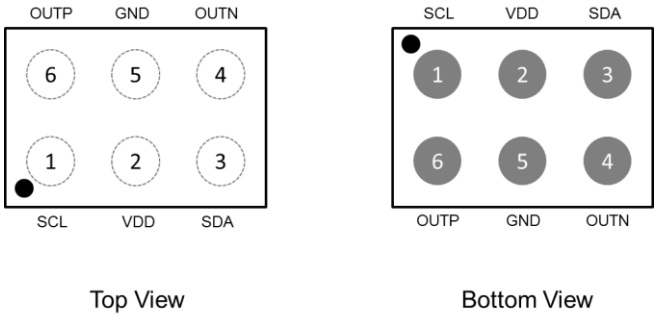

Figure 9 : Top and bottom view

6.2 Chip identifier

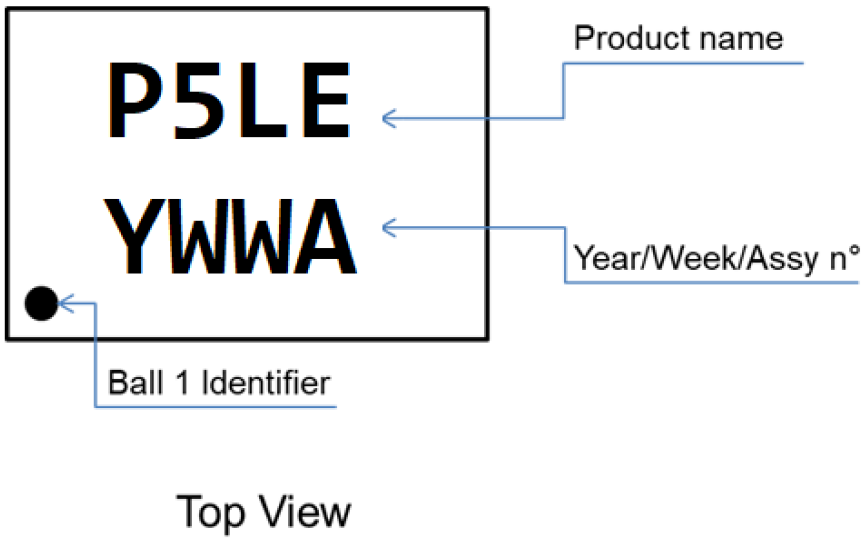

Figure 10 : chip identifier

7 Assembly

PD50LE is made using Amkor's WLCSP (Wafer Level Chip Scale Packaging) CSP^{nl} Bump on Repassivation technology. The technology is designed to utilize industry-standard surface mount assembly and reflow techniques. It is recommended to apply underfill after mounting.

8 Storage and shelf life

Recommended storage conditions for PD50: <30°C and <85°% RH. The product is classified as MSL1 device (Moisture Sensitivity Level 1) with unlimited shelf life if stored according to recommended conditions (ref. JEDEC J-STD-020 and JEDEC J-STD-033).

9 Restrictions of Hazardous Substances (RoHS)

PD50 is RoHS compliant.

poLight ASA reserves the right to alter without notice the datasheet, hereunder but not limited to the specification, design, price or conditions of supply of the product.